HARDWARE IMPLEMENTATION OF A DUAL TWO-LEVEL INVERTER WITH SVPWM USING PIC MICROCONTROLLER

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Abstract

Dual Two-Level Inverter is an emerging Multilevel Inverter Topology which is implemented by cascading two standard Two-Level inverters with a six-wire open-end load in between them. Space Vector PWM Technique is implemented considering its various advantages and is selected as a good performing control strategy to control the Dual-inverter. Dual Two-Level Inverter produces space vector locations, identical to those of a conventional Three-level inverter. It is well suited for automotive applications in which splitting the batteries bank is possible. Simulation of Dual Two-Level Inverter fed Induction motor is done in MATLAB and a hardware prototype of a Dual Two-Level Inverter fed open-end load is implemented with SVPWM using PIC16F877A Microcontroller and outputs obtained are presented.

Key Words : Dual Two-Level Inverter, Space Vector PWM

1. Introduction

Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control applications. The main advantages of multilevel inverters include increased number of voltage levels which leads to better voltage waveforms and reduced Total Harmonic Distortion (THD) in voltage, reduced switching stresses on the devices, Synthesis of higher voltage levels using power devices of lower voltage ratings. Among various multilevel inverter topologies, Three-Level Neutral Point Clamped (NPC) Inverters have found broad applications in high power drives. It offers features such as low THD, static voltage equalization without using additional components and no dynamic voltage sharing problem [1].

The proposed work is based on the Dual Inverter fed open-end load with conventional two-level inverters and hence does not experience neutral point fluctuations. It does not require the neutral point clamping diodes and has a simple power circuit. The proposed scheme uses half the dc-link voltage compared to the conventional Three-Level neutral point clamped inverter based scheme and has a lesser device count [2],[3],[4].

The dual Two-level inverter is composed of twelve switches and the possible states of the inverter depend on six variables which give the state of each leg. These variables can assume only two values and so the number of all the allowed configurations is obtained as 64 as equivalent to Three-Level Inverter.

2. Dual Two-level Inverter

![Fig. 1: Dual Two-Level Inverter fed Open-End Load](image)

The schematic of a Dual Two-Level inverter fed open-end load, where Inverter I and Inverter II are conventional two-level inverters is shown in Fig.1. A Dual Two-Level Inverter fed Open-End winding induction motor is obtained by opening the neutral point of the conventional cage induction motor and does not require any design change in the motor.

3. Space Vector PWM

Space vector Pulse Width modulation is a powerful PWM technique which treats the inverter as a single unit. The most important feature required for a well-designed PWM technique is that it should not allow different phases to switch simultaneously. It is the only PWM technique which satisfies the above condition. In SVPWM, the three phase sinusoidal voltages are represented using a single space vector. Using suitable transformations the three phase voltages are transformed to a single space vector in two dimensions. The important
condition to be satisfied while we synthesize a reference space vector is the volt-second balance principle. [5].

Some of the features of this method that have made it a very popular three-phase PWM generation method are:

1. It is inherently suitable for digital implementation.
2. It provides lower relative harmonic content compared to sinusoidal PWM.
3. The switching frequency of the inverter switches is half the carrier frequency. Therefore the switching losses are lesser compared to a sinusoidal PWM with same carrier frequency.
4. No pulses of opposite polarity in half cycle of line-line voltages waveforms and hence small ripple current.
5. Sub-harmonics (frequencies which are not integral multiples of fundamental) are zero. PWM waveforms are synchronized with its own fundamental and don’t allow different phases to switch simultaneously.
6. It provides more efficient use of supply voltage in comparison with sine PWM.

4. Simulation

Simulation of Dual Two-Level inverter fed induction motor is done in MATLAB. The inputs for the model shown in Fig.2 are the PWM signals of the individual inverters and their DC link voltages. Inverters are modeled using basic output voltage equations [6].

The pole voltages of the individual inverters are then computed. Subtracting the pole voltages of inverter-2 from those of inverter-1, the difference of pole voltages is obtained. The output of Dual Inverter is shown in Fig.3.

5. Hardware Implementation

A dual two-level inverter is designed using two standard two-level inverters. IGBT IRG4PH50UD is selected as the power switch for Dual inverter. Driver and isolation circuit is designed using TLP-250. SVPWM Pulses for the inverter is generated using PIC 16F877A Microcontroller. The proposed circuit configuration is implemented for a Three-phase Lamp Load with single power supply and was tested for low input voltage and output waveform patterns obtained are presented.

A. SVPWM Pulse generation using PIC 16F877A

PIC16F877A is one of the 8-bit micro-controller produced by Microchip Technology. This microcontroller is considered to be unique as it uses flash memory as its program memory and thus it can be programmed again and again without using ultra-violet to erase its program memory. The device consumes less power and operates at 5V. It has a relatively sufficient memory for storage purposes and industrial applications, and can also support high frequency, which is approximately up to a maximum of 20 MHz. PIC16F877A is a 40 pin IC with 33 I/O ports.

The complete algorithm for generating the SVPWM pulses is explained in Fig.4. The program would start with the acceptance of input parameters including magnitude and phase. Then generation of counter which involves degrees from 0° to 360° will be conducted. This counter will ensure that only a complete cycle is taken into consideration. Once the input phase has been identified, sector number would be chosen based on the phase angle of the input. Sector number is important to select the output waveform and equations to calculate the parameters. After that, interrupt would be activated to enable the calculation of parameters. This would be followed by obtaining the output waveform or binary code from a look-up table (assembly language) or an array (C language). With all those ready, interrupt would be deactivated and output waveform would be displayed based on the binary code and the values of parameters. The process is repeated when a new input is inserted into the program.
Fig. 4 : Flowchart of SVPWM Pulse Generation

The hardware results of SVPWM Pulses using PIC16F877A are shown in Fig.5 for Three-phase Two-Level inverter.

B. Driver Design (TLP250)

The major functions of driver circuit are amplification, isolation and level shifting. High side Switch of inverter legs requires isolated gate driver circuit as its source and control circuit grounds are at different points. TLP250 opto-coupler IC powered from 0-12V transformer is used to achieve isolated gate driver circuit. So as to keep circuit symmetry lower switches also are connected through TLP250 without isolation. The TOSHIBA TLP250 is an 8-pin IC consisting of a GaAlAs light emitting diode and an integrated photo-detector.

The complete circuit of TLP250 Driver with associated circuitry is shown in Fig.6. The hardware results of driver outputs are shown in Fig.7.

Selections of various components are carried as follows.

- \( R_1 = 330\Omega \)
- \( R_2 = 10\Omega \)
- \( R_3 = 1.2k \)
- \( C_1 = 100nF \)
- \( C_2 = 100\mu F \)
C. Dual inverter Design

A dual two-level inverter is designed using two standard two-level inverters. IGBT IRG4PH50UD is selected as the power switch for Dual inverter. SVPWM pulses for Inverter 1 are obtained at the six pins of port B (BO-B5) of PIC Microcontroller. The pulses for Inverter 2 is also taken from these pins in such a manner that the output voltage across R, Y and B phases are at 120 degree apart.

A (0-200V) rectifier circuit was designed to obtain DC input voltage from 230V single-phase AC. The output of rectifier circuit was supplied to the Dual Two-level Inverter. The complete hardware assembly of Dual Two-Level inverter fed open-end load is shown in Fig.8. The circuit was tested for low input voltage and the output waveforms obtained are verified.

The SVPWM pulses obtained using PIC Microcontroller was supplied to the two three-phase Two-Level inverters for verification. The results obtained are shown below. Fig.9 shows the phase outputs of Three-phase Two-Level inverter. We can observe that VRN and VYN are having 120 degree phase shift and its clear that VRN and VBN are having 240 degree phase shift. Fig.10 shows the line outputs of Two-level inverters.

Fig. 6 : Circuit Connection of TLP-250

Fig. 7 : Driver outputs for Inverter

Fig. 8 : Hardware assembly of Dual Two-Level Inverter fed open-end Load

Fig. 9 : (a) VRN and VYN

Fig. 9 : (b) VRN and VBN
The two inverters are modulated in such a manner that the SVPWM pulses obtained from PIC Microcontroller was supplied to both inverters for providing a 120 degree phase shift between the three output phases. A three-phase 24V lamp load was provided across the three output phases of Dual inverter and the output voltage of Dual Two-level inverter obtained is as shown in Fig.11.

5. Conclusion

Simulation of a Dual Two-level inverter fed induction motor Drive is done in MATLAB and concluded that the proposed scheme produce the same three-level inversion as that of a conventional Three-level inverter. The functional verification of proposed scheme was carried out in PIC 16F877A based hardware. The outputs obtained for a Dual Two-Level inverter were found to be similar to that of a Three-Level inverter and can be extended for higher levels. The implementation of the proposed configuration can be done in DSP/FPGA Platform to achieve the required switching frequency due to maximum operating speed limitation of PIC Microcontroller.

References


